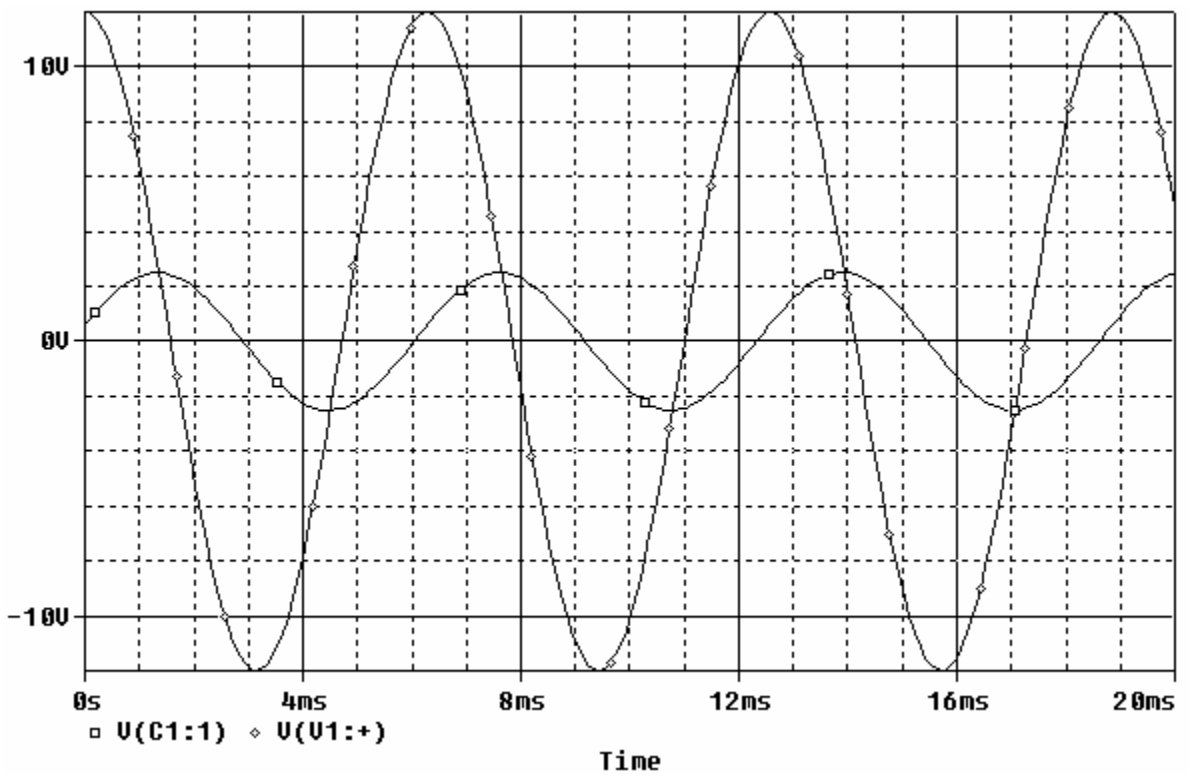
Front

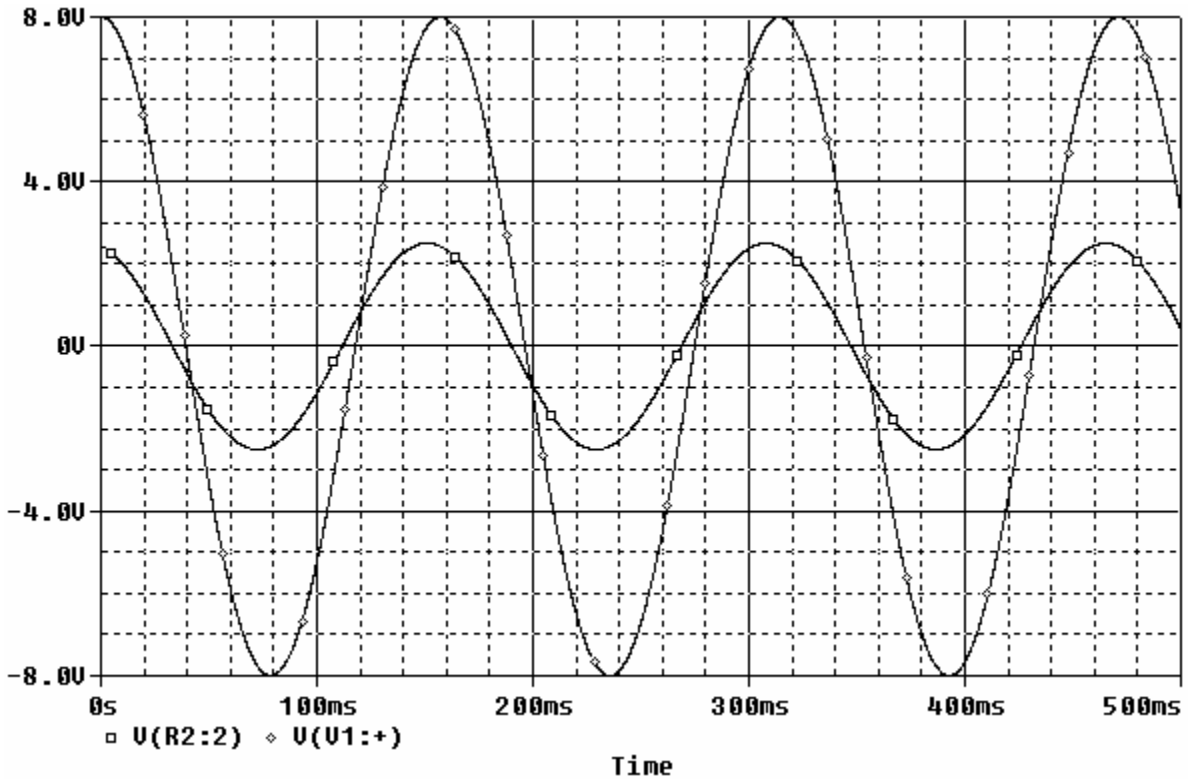
Design a circuit having one input, $v_i(t)$, and one output, $v_o(t)$. When the smaller of the sinusoids shown below is used as the input, the steady-state output must be the larger of the sinusoids.



Some points on the input plot: $v_i(0.00132) = 2.5$ V (max v_i) and v_i (0.00446) = -2.5 V (min v_i); v_i (0) = 0.6048 V.

Back

Design a circuit having one input, $v_i(t)$, and one output, $v_o(t)$. When the smaller of the sinusoids shown below is used as the input, the steady-state output must be the larger of the sinusoids.



Some points on the input plot: v_i (0.0722) = -2.5 V (min v_i) and v_i (0.151) = 2.5 V (max v_i); v_i (0) = 2.43 V.